

# BUFFER CIRCUIT, BUFFER TREE, AND SEMICONDUCTOR DEVICE

## FIELD OF THE INVENTION

[0001]

5       The present invention relates to a buffer circuit. More specifically, the invention relates to a buffer circuit suitably applied to a buffer for driving a clock signal and a semiconductor integrated circuit.

## BACKGROUND OF THE INVENTION

[0002]

10       Recently, in a semiconductor integrated circuit such as a high-speed CMOS circuit, an operating frequency become higher and hence one clock cycle is reduced. Further, as integration density and function level of a semiconductor integrated circuit become higher, a clock interconnection becomes longer. In a semiconductor integrated circuit  
15       provided with clock synchronous circuits such as latches or registers which perform sampling of data in response to a clock transition, a clock tree system is employed as a technique for matching delays from a clock source such as a clock input pin or an internal clock generation circuit to the respective clock synchronous circuits, thereby performing clock  
20       distribution. In the clock tree system, as shown in Fig. 12, clock buffer circuits (also referred to as "CTS (Clock Tree Synthesis) buffer circuits) INV101 to INV117 are disposed along clock propagation paths. A conventional clock buffer circuit is comprised of a PMOS transistor and an NMOS transistor. In case wherein the clock buffer circuit is  
25       composed of a CMOS inverter, an input signal is supplied to commonly

coupled gates of a PMOS transistor and an NMOS transistor connected in series between a high-potential power supply and a low-potential power supply, and an output signal of the clock buffer circuit is outputted from a connection point between a drain of the PMOS transistor and the drain of the NMOS transistor. For speeding up a high-level output driven by the PMOS transistor which is turned on, a size of the PMOS transistor is made large, while the size of the NMOS transistor is made small and hence a  $\beta_p/\beta_n$  ratio is made large, thereby achieving speeding up the high-level output, where the  $\beta_p/\beta_n$  ratio is a ratio of gain coefficients between the PMOS transistor and the NMOS transistor that constitute the CMOS inverter. The  $\beta$  is given by  $(\mu\epsilon/t_{ox})(W/L)$ , where  $\mu$  represents a carrier mobility,  $\epsilon$  represents a dielectric constant of a gate dielectric film,  $t_{ox}$  represents a thickness of the gate dielectric film,  $W$  represents a channel width, and  $L$  represents a channel length. However, when achieving the speeding up by increasing the  $\beta_p/\beta_n$  ratio, the size of the NMOS transistor must be made especially smaller because of a cell size constraint or the like, so that a fall time of an output waveform to a low level becomes slow. Further, if the  $\beta_p/\beta_n$  ratio is increased by reducing the size of the NMOS transistor, sensitivity to manufacturing variations is increased, as a result of which, an operation margin will be also extremely deteriorated.

[0003]

In Japanese Patent Kokai Publication JP-A-8-321768, a buffer circuit is disclosed that enabled a high-speed operation. In this buffer circuit, a charging circuit composed of a pMIS transistor and a

discharging circuit composed of an nMIS transistor are connected in series. An output of a rising-edge detection circuit for detecting a rising edge of an input signal is supplied to a gate of the pMIS transistor, while the output of a falling-edge circuit for detecting a falling edge of the input signal is supplied to the gate of the nMIS transistor. The output of a non-inverting gate for receiving the input signal is connected to the connection node between the pMIS transistor and the nMIS transistor. While one of the pMIS transistor and the nMIS transistor is turned on, the other is turned off, so that a short-circuit current does not flow through the nMIS and pMIS transistors, thereby enabling the high-speed operation. In the buffer circuit in the above-mentioned publication, the edge detection circuits are inserted between an input terminal and the gate of the pMIS transistor and between the input terminal and the gate of the nMIS transistor. Both rise and fall transitions of an output signal are delayed by times corresponding to respective propagation delays of the edge detection circuits and hence the circuit is unsuitable as a high-speed buffer circuit. In other words, in the buffer circuit described in the above-mentioned publication, in case wherein a clock synchronous circuit such as a latch or a register samples data by using only one of a rising edge and a falling edge of a clock signal, the clock signal edge used is delayed as with the clock signal edge not used.

#### SUMMARY OF THE DISCLOSURE

[0004]

If a propagation delay time of each buffer circuit inserted in a

clock path for delay adjustment is long and a plurality of buffer circuits are inserted from a clock source to a clock destination, delays caused by the buffer circuits greatly affect an operation timing of a clock synchronous circuit such as a latch or register, which is a clock destination. In a CMOS circuit driven with an operating frequency exceeding 100 MHz, for example, one clock cycle ( $t_{CK}$ ) is less than 10 nanoseconds. As shown in Fig. 12, four buffers for delay adjustment are inserted in each clock tree. If the propagation delay time per buffer is assumed to be roughly 600 ps (pico-seconds), 2.4 ns (nano-seconds) of time is spent for the buffers for delay adjustment and hence a sufficient timing margin in a latch, register or the like, which is the clock destination, may not be left.

[0005]

As described above, in order to ensure sufficient setup and hold times and operation of a latch or a register that operates in response to a clock, it is preferable that a delay time of the buffer circuit used for delay adjustment is short.

[0006]

Accordingly, it is an object of the present invention to provide a buffer circuit for reducing a delay time thereof and a semiconductor integrated circuit that uses the buffer circuit.

[0007]

The above and other objects are attained by a buffer circuit in accordance with an aspect of the present invention, which has an input terminal for receiving an input signal and an output terminal for

outputting an output signal, and which comprises:

a first transistor and a second transistor, connected in series between a first power supply and a second power supply having different power supply voltages, being controlled to be on and off based  
5 on signals fed to control terminals thereof,

a connection node between said first transistor and said second transistor being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

10 a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to be supplied to said control terminal of said second transistor, said control circuit performing control so that

15 when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply,  
20 said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to  
25 be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off.

[0008]

5 In the present invention, when a difference voltage between the voltage of the signal supplied to the control terminal of the first transistor and the voltage of the first power supply has exceeded the threshold voltage of the first transistor during transition of the input signal supplied to the control terminal of the first transistor from the  
10 first logic level to the second logic level, the first transistor is turned on with the second transistor kept off, and transition of the output signal voltage of the output terminal of the buffer circuit to the voltage of the first power supply is started.

[0009]

15 In the present invention, the control circuit includes a logic circuit for generating the signal to be supplied to the control terminal of the second transistor based on the result of a logical operation on the input signal supplied to the input terminal of the buffer circuit and the output signal outputted from the output terminal of the buffer circuit;  
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the logic circuit is configured to generate the signal at a logic level for turning on the second transistor and supply the signal to the control terminal of the second transistor when the input signal supplied to the input terminal of the buffer circuit is at the first logic level and  
25 the output signal outputted from the output terminal of the buffer circuit

is at the first logic level, and

then to generate the signal at a logic level for turning off the second transistor and supply the signal to the control terminal of the second transistor when the second transistor is then turned on and the output signal outputted from the output terminal of the buffer circuit becomes the second logic level.

[0010]

The present invention includes:

a flip-flop circuit with an input terminal thereof connected to the output terminal of the buffer circuit, for storing and holding the logic level of the output signal of the buffer circuit and outputting a signal storing and holding the logic level from an output terminal thereof; wherein the output terminal of the flip-flop circuit is connected to the output terminal of the buffer circuit.

[0011]

In the present invention, the control circuit comprises:

an inverter having an input terminal for receiving the input signal supplied to the input terminal of the buffer circuit and an output terminal for outputting the inverted signal of the input signal; and

a logic circuit for receiving at two input terminals thereof a signal at a logic level inverted from the logic level of the output signal of the output terminal of the buffer circuit and stored and held in the flip-flop circuit and the output signal from the inverter and outputting the signal at the logic level for turning on the second transistor to the control terminal of the second transistor from an output terminal thereof when

the signals received at the two input terminals are both at the second logic level.

[0012]

In other aspect of the present invention, it may also be so  
5 configured that the control circuit receives a selection control signal for  
controlling activation and deactivation of the buffer circuit and includes  
means for outputting the signal at a logic level for turning off the second  
transistor when the selection control signal indicates a value  
commanding deactivation of the buffer circuit, thereby allowing control  
10 over activation and deactivation of the buffer circuit. As clear from  
descriptions given below, the above-mentioned object is likewise  
achieved by the inventions defined in the claims as well.

Still other objects and advantages of the present invention will  
become readily apparent to those skilled in this art from the following  
15 detailed description in conjunction with the accompanying drawings  
wherein only the preferred embodiments of the invention are shown and  
described, simply by way of illustration of the best mode contemplated  
of carrying out this invention. As will be realized, the invention is  
capable of other and different embodiments, and its several details are  
20 capable of modifications in various obvious respects, all without  
departing from the invention. Accordingly, the drawing and description  
are to be regarded as illustrative in nature, and not as restrictive.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a first  
25 embodiment of the present invention;



Fig. 2 is a waveform diagram for explaining input and output operations of the first embodiment of the present invention;

Fig. 3 is a timing chart of an input signal and an output signal for explaining an overview of the first embodiment of the present invention;

5 Fig. 4 is a timing chart for explaining an operation of the first embodiment of the present invention;

Fig. 5 is a block diagram showing a configuration of a second embodiment of the present invention;

10 Fig. 6 is a timing chart of the input signal and the output signal for explaining an overview of the second embodiment of the present invention;

Fig. 7 is a timing chart for explaining an operation of the second embodiment of the present invention;

15 Fig. 8 is a block diagram showing a third embodiment of the present invention;

Fig. 9 is a block diagram showing a configuration of a fourth embodiment of the present invention;

Fig. 10 is a timing chart for explaining an operation of the fourth embodiment of the present invention;

20 Fig. 11 is a block diagram showing a configuration of a delay circuit according to the fourth embodiment of the present invention;

Fig. 12 is a block diagram showing a configuration of clock trees to which buffer circuits according to the embodiments of the present invention are applied;

25 Fig. 13 is a graph showing a transient analysis simulation result

of clock tree buffers that used the third embodiment of the present invention;

Fig. 14 is a graph showing the transient analysis simulation result of clock tree buffers that used CMOS inverters as a comparison example;

5 Fig. 15 is a block diagram showing a configuration of a fifth embodiment of the present invention; and

Fig. 16 is a block diagram showing a configuration of a sixth embodiment of the present invention.

#### PREFERRED EMBODIMENTS OF THE INVENTION

10 [0013]

Preferred embodiments of the present invention will be described below. A buffer circuit according to an embodiment of the present invention includes first and second transistors (PM1 and NM1) connected in series between a first power supply that is a high-potential power supply (VDD) and a second power supply that is a low-potential power supply (VSS), and a connection node between the first transistor and the second transistor is an output terminal (OUT) of the buffer circuit. A control terminal of the first transistor (PM1) is connected to an input terminal (IN) of the buffer circuit. The first transistor is  
15 turned off when a signal supplied to the input terminal (IN) is at a first logic level (high) which corresponds to a first power supply voltage (VDD), and is turned on when the signal is at a second logic level (low) which corresponds to a second power supply voltage (VSS). The first transistor (PM1) is turned on when a difference voltage ( $= |V_{IN} - V_{DD}|$ )  
20 between a voltage ( $V_{IN}$ ) of the signal supplied to a control terminal  
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thereof and the first power supply voltage (VDD) exceeds a threshold voltage  $|V_{tp}|$  of the first transistor (PM1), and causes an output signal voltage of the output terminal (OUT) of the buffer circuit to undergo a transition to the first power supply voltage (VDD).

5 [0014]

One of main features of the present invention is that the invention includes a control circuit for performing control so that when an input signal supplied to the input terminal (IN) of the buffer circuit has changed from the first logic level to the second logic level and then the first transistor (PM1) having a control terminal for receiving the input  
10 signal is switched from off to on, the second transistor (NM1) is kept off.

[0015]

More specifically, the control circuit receives the input signal supplied to the input terminal (IN) of the buffer circuit and outputs a  
15 signal to be supplied to the control terminal of the second transistor (NM1). The control circuit performs control so that when the input signal is at the second logic level (low), the control circuit supplies the signal at a logic level for turning off the second transistor (NM1) to the control terminal of the second transistor (NM1), and when the input  
20 signal is at the first logic level (high), the control circuit supplies to the control terminal of the second transistor (NM1) the signal for turning on the second transistor (NM1) to cause the voltage of the output terminal (OUT) of the buffer circuit to undergo a transition to the second power supply voltage (VSS) and then setting the second transistor (NM1) to be  
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off before the input signal undergoes a transition from the first logic level to the second logic level.

[0016]

In the embodiment of the present invention having an above  
5 configuration, at a time point when the voltage ( $V_{IN}$  of the input signal supplied to the input terminal (IN) of the buffer circuit changes from the first supply voltage (VDD) to  $VDD - |V_{tp}|$  or lower and the first transistor (PM1) is switched from off to on, the second transistor (NM1) is kept off. Thus, even when the first transistor (PM1) has been turned  
10 on, no short-circuit current flows from the first power supply (VDD) to the second power supply (VSS). Then, in this state, charging of the output terminal (OUT) by a drain current of the first transistor (PM1) is started. With this arrangement, a propagation delay time  $t_{pLH}$  from a fall (transition from a high level to a low level) of the input signal to a  
15 rise (transition from the low level to the high level) of the output signal of the buffer circuit is reduced more than in a buffer circuit of a ordinary CMOS inverter configuration composed of the first transistor (PM1) and the second transistor (NM1).

[0017]

20 Further, in this embodiment, as an input load (a gate capacitance) seen from the input terminal (IN) of the buffer circuit, only the input load (gate capacitance) on the control terminal of the first transistor (PM1) can substantially be seen. In other words, in the control circuit for generating the signal for controlling on/off of the second transistor  
25 (NM1), the input load (gate capacitance) on a circuit for receiving the

input signal supplied to the input terminal (IN) of the buffer circuit, (such as an inverter INV1 in Fig. 1), is considerably smaller than the input load on the control terminal of the first transistor (PM1). For this reason, a fall time of the input signal applied to the input terminal  
5 (IN) of the buffer circuit is also reduced, consequently contributing to a reduction in the propagation delay time  $t_{pLH}$  of the buffer circuit.

[0018]

Generally, in a buffer circuit for driving a heavy load, in order to have a high current-driving capability, a gate width (W) of an output  
10 transistor is set to be large. For this reason, the input load (gate capacitance) of the buffer circuit becomes large. When the gates of the PMOS transistor and the NMOS transistor are commonly connected to the input terminal (IN) of the buffer circuit, as in an ordinary CMOS inverter configuration, the gate capacitances of the two transistors are  
15 connected in parallel, as seen from the input terminal (IN), so that the input load capacitance is nearly doubled, compared with a case in the present embodiment.

[0019]

In the present embodiment, the second transistor (NM1) is turned  
20 on when the input signal from the input terminal (IN) of the buffer circuit has changed from the second logic level (low) to the first logic level (high). When the input signal supplied to the input terminal (IN) of the buffer circuit is at the second logic level, the first transistor (PM1) is in an on state. When the input signal has changed from the  
25 second logic level (low) to the first logic level (high), the first logic

level (high) is supplied to the control terminal of the second transistor (NM1), being delayed with a delay time of the control circuit for controlling on/off of the second transistor (NM1), and then the second transistor (NM1) is turned on. At this time, the first logic level (high) is supplied to the control terminal of the first transistor (PM1) from the input terminal (IN) of the buffer circuit, so that the first transistor (PM1) is kept off. Thus, when the second transistor (NM1) is switched from off to on, the short-circuit current does not flow from the first power supply (VDD) to the second power supply (VSS), thereby achieving a reduction in power consumption. Further, when the second transistor (NM1) is turned on, the short-circuit current does not flow. Thus, a speed up of a fall time of the output signal from the output terminal in the buffer circuit is achieved.

[0020]

In this embodiment, a propagation delay time  $t_{pHL}$ , which is a delay time from a rise transition of the input signal supplied to the input terminal (IN) of the buffer circuit to a fall transition of the signal of the output terminal (OUT) of the buffer circuit, is not reduced, as distinct from the above-mentioned  $t_{pLH}$  which is a propagation delay time from a fall transition of the input signal to a rise transition of the signal of the output terminal (OUT) of the buffer circuit, and which is reduced by speeding up a start of the transition. In other words, the signal of the output terminal (OUT) of the buffer circuit falls from the first logic level (high) to the second logic level (low), being delayed by a delay time during which the input signal passes through the control circuit.

[0021]

When the input signal supplied to the input terminal (IN) of the buffer circuit has changed from the second logic level (low) to the first logic level (high), the first transistor (PM1) is switched off, and the second transistor (NM1) is turned on once, being delayed by the delay time of the control circuit. A signal voltage of the output terminal (OUT) is changed to the second logic level corresponding to the second power supply voltage (VSS) from the first power supply voltage (VDD). Thereafter, the second logic level (low) is supplied to the control terminal of the second transistor (NM1), so that the first and second transistors both are turned off. The output terminal of the buffer circuit thus is in a high-impedance state.

[0022]

At this time, a flip-flop circuit, which is connected to the output terminal (OUT) of the buffer circuit and is composed of two inverters (INV2 and INV3), with input terminals thereof being connected to an output terminal of others, stores and holds the logic level of the output terminal (OUT) of the buffer circuit, immediately before the output terminal (OUT) of the buffer circuit is set in the high-impedance state. The output terminal (OUT) of the buffer circuit in the high-impedance state is set to the logic level outputted from the inverter (INV3) at a flip-flop output stage. That is, when the input signal supplied to the input terminal (IN) of the buffer circuit has changed from the second logic level (low) to the first logic level (high), the second transistor (NM1) is turned on once. Then, even if the second transistor (NM1) is

turned off during a time before a change of the input signal from the first logic level (high) to the second logic level (low), the voltage of the output terminal (OUT) of the buffer circuit is pulled up or pulled down to the original logic level via the output terminal of the inverter (INV3) which composes the flip-flop output stage. In other words, in this embodiment, even if the output terminal of the buffer circuit is kept in the high-impedance state, its output voltage is avoided from remaining at a voltage intermediate between the first logic level (high: VOH) and the second logic level (low: VOL) or being set to a logic level different from the original logic level.

[0023]

As another embodiment of the present invention, in the buffer circuit according to the above-mentioned embodiment, the first power supply may be replaced with the low-potential power supply (VSS), the second power supply may be replaced with the high-potential power supply (VDD), and thus the first logic level corresponding to the first power supply voltage and the second logic level corresponding to the second power supply voltage may be changed to low and high, respectively. In this another embodiment, of the two transistors (PM1 and NM1) connected in series between the first power supply (VSS) and the second power supply (VDD), the transistor over which on/off switching control is performed by the control circuit is replaced with the transistor (PM1), and the propagation delay time  $t_{pHL}$  from a rise transition of an input signal supplied to the input terminal (IN) of the buffer circuit to a fall transition of an output signal of the output



terminal (OUT) of the buffer circuit is reduced. That is, in this another embodiment, the first transistor having a control terminal directly connected to the input terminal (IN) of the buffer circuit is the NM1 in Fig. 1, while the second transistor which is controlled to be on and off by a signal supplied to its control terminal from the control circuit is the PM1 in Fig. 5, the transistors being interchanged as compared with those in the before-mentioned embodiment described with reference to Fig. 1. Another embodiment of the present invention will be described below with reference to Fig. 5.

10 [0024]

More specifically, another embodiment includes the first and second transistors (NM1 and PM1) connected in series between the first power supply (VSS) and the second power supply (VDD), and the connection node between an output of the first transistor and the output of the second transistor is the output terminal (OUT) of the buffer circuit. The control terminal of the first transistor (NM1) is connected to the input terminal (IN) of the buffer circuit. When the difference voltage  $V_{IN} - V_{SS}$  between the voltage ( $V_{IN}$ ) of a signal supplied to the control terminal of the first transistor (NM1) and the first power supply voltage ( $V_{SS}$ ) exceeds a threshold voltage ( $V_{tn}$ ) of the first transistor (NM1), the first transistor (NM1) is turned on to cause the output terminal (OUT) of the buffer circuit to undergo a transition to the first power supply voltage ( $V_{SS}$ ). One of the main features of the another embodiment of the present invention is that this embodiment has a control circuit for performing control so that when the first transistor

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(NM1) is switched from off to on, the second transistor (PM1) is kept off.

[0025]

This control circuit comprises a circuit for receiving the input  
5 signal supplied to the input terminal (IN) of the buffer circuit and for  
outputting a signal to be supplied to the control terminal of the second  
transistor (PM1). When the input signal is at the second logic level  
(high) corresponding to the second power supply voltage (VDD), the  
control circuit supplies the signal for turning off the second transistor  
10 (PM1) to the control terminal of the second transistor (PM1). The  
control circuit sets the signal to be supplied to the control terminal of  
the second transistor (PM1) so that when the input signal is at the first  
logic level (low) corresponding to the first power supply voltage (VSS),  
the second transistor (PM1) is turned on to cause the voltage of the  
15 output terminal (OUT) of the buffer circuit to undergo a transition to the  
second power supply voltage (VDD) and then the second transistor  
(PM1) is turned off.

[0026]

In another embodiment of the present invention, when the input  
20 signal supplied to the input terminal (IN) of the buffer circuit has  
changed from the first logic level (low) to the second logic level (high)  
and then the first transistor (NM1) is switched from off to on, the second  
transistor (PM1) is kept off. Thus, even when the first transistor  
(NM1) is turned on, no short-circuit current from the power supply  
25 (VDD) to the power supply (VSS) flows, and the output terminal (OUT)

is discharged through the first transistor (NM1) in the on state. Thus, the propagation delay time  $t_{pHL}$  from a rise of the input signal (transition to the high level) to a fall of the output signal of the buffer circuit (transition to the low level) is reduced.

5 [0027]

Further, in this another embodiment, as the input load seen from the input terminal, only the input load (gate capacitance load) on the control terminal of the first transistor (NM1) is seen. Thus, the fall time of the input signal to the input terminal (IN) of the buffer circuit is also reduced, thus contributing to a reduction in the propagation delay time  $t_{pHL}$  of the buffer circuit. In this embodiment, the second transistor (PM1) is turned on when the input signal from the input terminal (IN) of the buffer circuit has changed from the second logic level (high) to the first logic level (low). When the input signal from the input terminal (IN) of the buffer circuit is at the second logic level (high), the first transistor (NM1) is in the on state. When the input signal changes from the second logic level (high) to the first logic level (low), the first logic level (low) is supplied to the signal for controlling the second transistor (PM1), being delayed by the delay time of the control circuit for controlling on/off of the second transistor (PM1), and then the second transistor (PM1) is turned on. At this time, the first logic level (low) is supplied to the control terminal of the first transistor (NM1) from the input terminal (IN) of the buffer circuit, so that the first transistor (NM1) is kept off. Thus, when the second transistor (PM1) is switched from off to on, the short-circuit current does not flow from the

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power supply (VDD) to the power supply (VSS) and hence the power consumption is reduced.

[0028]

In this another embodiment, in response to transition of the input  
5 signal supplied to the input terminal (IN) of the buffer circuit from the  
second logic level (high) to the first logic level (low), the second  
transistor (PM1) is turned on, being delayed by the delay time of the  
control circuit, so that the signal of the output terminal (OUT) of the  
buffer circuit changes from the first logic level (low) to the second logic  
10 level (high). When the input signal changes from the second logic  
level (high) to the first logic level (low), the first transistor (NM1) is  
turned off, while the second transistor (PM1) is turned on. Thus, the  
output terminal (OUT) is changed from the first logic level to the second  
logic level. Thereafter, before the input signal undergoes a transition  
15 from the first logic level (low) to the second logic level (high), the  
second logic level (high) is supplied to the control terminal of the  
second transistor (PM1) from the control circuit. Thus, the first and  
second transistors (NM1 and PM1) both become the off state, so that the  
output terminal of the buffer circuit becomes the high-impedance state.  
20 At this point, the flip-flop circuit (inverters INV2 and INV3 with their  
input terminals and output terminals interconnected) connected to the  
output terminal of the buffer circuit holds and outputs the logic level of  
the output terminal of the buffer circuit immediately before the output  
terminal of the buffer circuit becomes the high-impedance state. The  
25 output terminal of the buffer circuit in the high-impedance state is set to

a voltage corresponding to the original logic level of the buffer circuit to be outputted, by the output of the flip-flop (output of the inverter INV3).

[0029]

5           In other embodiment of the present invention, a control circuit includes the inverter (INV1) with an input terminal for receiving an input signal supplied to the input terminal of a buffer circuit and an output terminal for outputting an inverted signal of the input signal. The control circuit receives the output of the inverter (INV2)  
10   constituting the flip-flop circuit, the output of the inverter (INV1), and a selection control signal or its inverted signal for controlling activation and deactivation of the buffer circuit at its three input terminals. The control circuit includes a logic circuit (NOR3). When the selection control signal indicates a value for commanding activation  
15   of the buffer circuit and the signals input to the three input terminals are all at the second logic level, the logic circuit (NOR3) outputs a signal at a logic level for turning on the second transistor (NM1) to the control terminal of the second transistor from its output terminal. When the selection control signal commands deactivation of the buffer circuit, the  
20   logic circuit (NOR3) outputs the signal at a logic level for turning off the second transistor to the control terminal of the second transistor from its output terminal, irrespective of the values of other two input signals. The present invention with an above-mentioned configuration can control supply and stop of a clock, while maintaining high-speed  
25   supply of a high level output. The buffer circuits in the embodiments

described above may of course also be combined for use as a configuration of the present invention.

[0030]

In order to describe the above-mentioned embodiments of the present invention in further detail, embodiments of the present invention will be described below with reference to drawings. Fig. 1 is a block diagram showing a configuration of a buffer circuit according to an embodiment of the present invention. Referring to Fig. 1, the buffer circuit in this embodiment is formed by using a CMOS process. This circuit is an inverting buffer circuit that receives an input signal supplied to an input terminal IN and outputs an inverted signal of the input signal from an output terminal OUT. The circuit includes a p-channel MOS transistor (referred to as a "PMOS transistor") PM1 with its source connected to a high-potential power supply VDD and an N-channel MOS transistor (referred to as an "NMOS transistor") NM1 with its source connected to a low-potential power supply VSS, and a connecting node between a drain of the PMOS transistor PM1 and the drain of the NMOS transistor NM1 is the output terminal OUT of the buffer circuit.

[0031]

A gate of the PMOS transistor PM1 is connected to the input terminal IN of the buffer circuit. When the input signal supplied to the input terminal IN is at a high level, the PMOS transistor PM1 is turned off. When an input signal voltage falls to be equal to or less than a value which is obtained by subtracting an absolute value  $|V_{tp}|$  for a

threshold voltage from a power supply voltage VDD, or  $VDD - |V_{tp}|$ , the PMOS transistor PM1 is turned on. Then, the PMOS transistor PM1 charges the output terminal OUT through the power supplies VDD, and causes the output terminal OUT to undergo a transition to the power supply voltage VDD. In other words, the output signal rises from a low level to a high level.

[0032]

An inverter INV1 and an NOR circuit NOR1 which receives an output of the inverter INV1 at one of input terminals are inserted between the input terminal IN of the buffer circuit and the gate of the NMOS transistor NM1. The inverter INV1 and NOR circuit NOR1 compose a control circuit for generating and outputting a signal to be supplied to the gate of the NMOS transistor NM1.

[0033]

When the input signal supplied to the input terminal IN is at a low level, the control circuit causes the NMOS transistor NM1 to be in an off state. When the input signal undergoes a transition to a high level, the control circuit causes the NMOS transistor to be turned on, causes electric charge at the output terminal OUT to be discharged to a side of the power supply voltage VSS, and then causes a voltage of the output terminal OUT to undergo a transition to the power supply voltage VSS. Thereafter, before the input signal falls from high to low, the control circuit sets the gate of the NMOS transistor NM1 to a low level. With this arrangement, at a time when the input signal undergoes a transition from a high level to a low level and the PMOS transistor PM1 is

switched from off to on, the NMOS transistor NM1 is kept off.

[0034]

In the present embodiment, when the PMOS transistor PM1 is switched from off to on, at a fall transition of the input signal, no short-circuit current from the power supply VDD to the power supply VSS flows.

[0035]

Referring to Fig. 1, a connection point between the drain of the PMOS transistor PM1 and the drain of the NMOS transistor NM1 is connected to the output terminal OUT of the buffer circuit, and is also connected to the input terminal of an inverter INV2 and the output terminal of an inverter INV3. The output terminal of the inverter INV2 is connected to the input terminal of the inverter INV3. The inverters INV2 and INV3 compose a flip-flop, which stores and holds a logic value for the output terminal OUT of the buffer circuit.

[0036]

Then, the output terminal of the inverter INV1, the input terminal of which is connected to the input terminal IN and the output terminal of the inverter INV2 are connected to the input terminals of the two-input NOR circuit NOR1. The output terminal of the NOR circuit NOR1 is connected to the gate of the NMOS transistor NM1.

[0037]

Fig. 2 is a waveform diagram showing an operation of a first embodiment of the present invention. Referring to Fig. 2, at a time point ( $t_0$ ) when an input signal voltage  $V_{IN}$  of the input terminal IN has



become equal to or lower than  $V_{DD}-|V_{tp}|$ , where the  $V_{tp}$  is the threshold voltage of the PMOS transistor PM1, an output signal voltage  $V_{OUT}$  of the output terminal OUT begins to rise.

[0038]

5           On contrast therewith, in a CMOS inverter (for a comparison example), composed of a PMOS transistor and an NMOS transistor connected in series between the power supplies  $V_{DD}$  and  $V_{SS}$ , which commonly receive the input signal at their gates and in which a connection point between their drains is connected to the output  
10 terminal, when the input signal voltage  $V_{IN}$  undergoes a transition to be equal to or lower than  $V_{DD}-|V_{tp}|$ , the PMOS transistor is turned on and the NMOS transistor, however, is also in an on state. Accordingly, the short-circuit current flows from the power supply  $V_{DD}$  to the power supply  $V_{SS}$  through the PMOS transistor and NMOS transistor that are  
15 in the on state. When the input signal voltage becomes lower than  $V_{tn}$ , where  $V_{tn}$  is the threshold voltage of the NMOS transistor, the NMOS transistor is turned off. Thus, the short-circuit current flows from the power supply  $V_{DD}$  to the power supply  $V_{SS}$  during a period in which the input signal voltage is in the range between the  $V_{DD}-|V_{tp}|$  and  $V_{tn}$ .  
20 Accordingly, in the comparison example, when the input signal to the CMOS inverter changes from a high level to a low level, a start time of a rise of the output signal is delayed, as shown in a dotted line (in the comparison example) in Fig. 2, from the embodiment of the present invention.

25           [0039]

As described above, in the present invention, a propagation delay time  $t_{pLH}$  from high to low transition of the input signal to low to high transition of the output signal is made more reduced than that of the CMOS inverter.

5 [0040]

In the CMOS inverter, it is necessary to drive parallel gate load capacitances of the PMOS transistor and the NMOS transistor. On contrast therewith, in the present invention, as a gate load seen from the input terminal IN, there is only a gate capacitance of the PMOS transistor in the buffer circuit. That is, the inverter INV1 may be the one just for generating a signal for supply to the NOR 1, and does not drive a load such as a clock interconnection, as being distinct from the PMOS transistor PM1 and the NMOS transistor NM1. Thus, a device size of the inverter INV1 can be made smaller than the PMOS transistor and hence, as the gate load seen from the input terminal IN, only the gate capacitance of the PMOS transistor in the buffer circuit is seen, which contributes to high-speed transition of the input signal.

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[0041]

Fig. 3 is a timing chart schematically showing an example of an input signal to the input terminal (IN) and an output signal from the output terminal (OUT) in the buffer circuit in the first embodiment of the present invention. As shown in Fig. 3, in this embodiment, the propagation delay time  $t_{pLH}$  from a fall of the input signal supplied to the input terminal (IN) of the buffer circuit to a rise of the output signal of the output terminal (OUT) of the buffer circuit is reduced more than

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in an ordinary CMOS inverter. In this embodiment, a propagation delay time  $t_{pHL}$  from a rise of the input signal to a fall of the output signal is behind that of the ordinary CMOS inverter by a delay time specified by the propagation delays of the inverter INV1 and the NOR circuit NOR1 in Fig. 1.

[0042]

Fig. 4 is a timing chart for explaining an operation of the buffer circuit in the first embodiment of the present invention shown in Fig. 1. Referring to Fig. 4, IN denotes a signal waveform at the input terminal, A denotes a signal waveform at a node for the gate of the PMOS transistor PM1, B denotes a signal waveform at the node for the output of the inverter INV1 (a first input to the NOR1), C denotes a signal waveform at the node for the gate of the NMOS transistor NM1, D denotes a signal waveform at the node for the connection point between the drains of the PMOS transistor PM1 and the NMOS transistor NM1, and E denotes a signal waveform at the node for the output of the inverter INV2 (a second input to the NOR1), in Fig. 1.

[0043]

When the input signal IN rises (at a timing  $T_0$  in Fig. 4), the node B falls to a low level, with a delay by the delay time of the inverter INV1. At this time, the node D is at a high level and the node E is at a low level. Thus, the node C for the output of the NOR circuit NOR1 undergoes a transition from a low level to a high level. In response to a rise of the node C, the NMOS transistor NM1 that receives the voltage at the node C as a gate voltage is switched from off to on, and discharges

electric charge at the node D to the VSS side to cause the node D to undergo a transition to a low level. When the NMOS transistor NM1 is switched on from off, a high level is applied to the node A or the gate of the PMOS transistor PM1, so that the PMOS transistor PM1 is in the off state. Thus, the short-circuit current from the power supply VDD to the power supply VSS does not flow.

[0044]

When the node D falls to a low level, the node E, which is the output node of the inverter INV2, goes to a high level and the node C, which is the output node of the NOR circuit NOR1 which receives a voltage of node E, goes to a low level.

[0045]

When the node C goes to a low level, the NMOS transistor NM1, which receives the voltage at the node C as the gate voltage is turned off. During this period as well, the input signal are high, and the PMOS transistor PM1 is in the off state. The PMOS transistor PM1 is in the off state until the input signal IN undergoes a transition from high to low. During a period indicated by  $T_{off}$  (the period from a fall timing of the node C to a fall timing of the input signal IN), the output terminal OUT in the buffer circuit is made in a high-impedance state.

[0046]

The flip-flop composed of the inverters INV2 and INV3 stores and holds the logic value for the node D (logic value before the high-impedance state). During the period ( $T_{off}$ ) where the output terminal OUT of the buffer circuit is in the high-impedance state, the inverter

INV3, the output terminal of which is at a low level, discharges the output terminal OUT of the buffer circuit, and functions to cause the output terminal OUT of the buffer circuit to be at a low level. The inverter V3 is composed of a CMOS inverter, and preferably, the size of a NMOS transistor of the CMOS inverter is smaller than that of the NMOS transistor NM1 composing the buffer circuit. During the period ( $T_{off}$ ) where both of the PMOS transistor PM1 and the NMOS transistor NM1 in the buffer circuit are in an off state, if the output signal voltage of the output terminal (OUT) is at a low level (of a VOL or lower, or close to the VOL) and does not reach the power supply voltage VSS yet, the inverter INV3 that outputs the low level causes the output signal voltage of the output terminal (OUT) to fall to the power supply voltage VSS.

[0047]

When the input signal IN falls at a timing  $T_A$  in Fig. 4, the PMOS transistor PM1 which is switched from off to on starts charging the output terminal OUT (node D) through the power supply VDD, and a transition of the output terminal OUT (node D) to a high level is immediately started, as described with reference to Fig. 2. The node E at this time changes to a low level, the node B is set to a high level, and the node C which is the output node of the NOR circuit NOR1 is kept at a low level. That is, the NMOS transistor NM1 is kept off.

[0048]

Incidentally, in Fig. 4, a transition timing of a clock signal supplied to the input terminal (IN) of the buffer circuit from a high level

to a low level between timings  $T_0$  and  $T_1$  is indicated by  $T_A$ , and a duty ratio of the clock signal supplied to the input terminal (IN) of the buffer circuit is set to 1:1 (50%), for simplicity. In this embodiment, the duty ratio of the clock signal may, of course, be other than 1:1. In Fig. 4, a  
5 period from the timing  $T_0$  to the timing  $T_1$  constitutes one clock cycle (tCK).

[0049]

Next, a second embodiment of the present invention will be described. Fig. 5 is a block diagram showing a configuration of the  
10 second embodiment of the present invention. Referring to Fig. 5, this embodiment is obtained by interchanging polarities of the transistors where the signals input to the gates are controlled, as compared with those in the before-mentioned embodiment. In the present embodiment, the input signal fed to the input terminal IN is fed to the gate of the  
15 NMOS transistor NM, while the output signal of a control circuit constituted from the inverter INV1 and a NAND circuit NAND1 is fed to the gate of the PMOS transistor PM1. In the before-mentioned embodiment, the propagation delay time from a fall of the input signal to a rise of the output signal of the buffer circuit to was reduced. In the  
20 present embodiment, the propagation delay time  $t_{pHL}$  from a rise of the input signal to a fall of the output signal of the buffer circuit is reduced, as shown in Fig. 6.

[0050]

More specifically, referring to Fig. 5, the buffer circuit in the  
25 present embodiment includes a PMOS transistor PM1, which has a

source connected to the high-potential power supply VDD, and a NMOS transistor NM1 which has a source connected to the low-potential power supply VSS. The connection node between the drains of the PMOS transistor PM1 and the NMOS transistor NM1 is the output terminal OUT of the buffer circuit. The gate of the NMOS transistor NM1 is connected to the input terminal IN of the buffer circuit. When the input signal is at a low level, the NMOS transistor NM1 is in an off state. When the input signal voltage rises to exceed the threshold voltage  $V_{tn}$  of the NMOS transistor NM1, the NMOS transistor NM1, which is turned on, discharges the output terminal OUT of the buffer circuit and causes output terminal OUT to undergo a transition to the power supply voltage VSS.

[0051]

A circuit composed of an inverter INV1 and a NAND circuit NAND 1 is inserted between the input terminal IN of the buffer circuit and the gate of the PMOS transistor PM1. The circuit constitutes the control circuit for controlling a timing of a signal to be supplied to the gate of the PMOS transistor PM1.

[0052]

When the input signal fed to the input terminal IN is at a high level, the control circuit causes the PMOS transistor PM1 to be turned off. When the input signal goes to a low level, the control circuit causes the PMOS transistor PM1 to be turned on to charge the output terminal OUT to the VDD and to set the output terminal OUT to a high level. Thereafter, the control circuit sets the gate of the PMOS

transistor PM1 to be at a high level. By doing so, when the input signal undergoes a transition from a low level to a high level, and the NMOS transistor NM1 is switched from off to on, the PMOS transistor PM1 is kept off. With this arrangement, the short-circuit current from the power supply VDD to the power supply VSS through the PMOS transistor PM1 and the NMOS transistor NM1 does not flow when the NMOS transistor NM1 is turned on.

[0053]

Referring to Fig. 5, the connection point between the drains of the PMOS transistor PM1 and the NMOS transistor NM1 is connected to a flip-flop composed of inverters INV2 and INV3, where an input of one inverter is connected to the output of the other inverter. The output of the inverter INV1 that has an input terminal connected to the input terminal IN and the output terminal of the inverter INV2 are connected to the input terminals of the NAND circuit NAND1. The output terminal of the NAND circuit NAND1 is connected to the gate of the PMOS transistor PM1.

[0054]

Fig. 7 is a chart for explaining an operation of the second embodiment of the present invention shown in Fig. 5. Referring to Fig. 7, IN denotes a signal waveform at the input terminal, A denotes the signal waveform at a node for the gate of the NMOS transistor NM1, B denotes a signal waveform at the node for the output of the inverter INV1 (first input to the NAND1), C denotes a signal waveform at the node for the gate of the PMOS transistor PM1, D denotes a signal



waveform at the node for the connection point between drains of the PMOS transistor PM1 and the NMOS transistor NM1, and E denotes a signal waveform at the node for the output of the inverter INV2 (second input to the NAND1), in Fig. 5.

5 [0055]

When the input signal rises at the timing  $T_0$  in Fig. 7, the NMOS transistor NM1 is turned on to make the output terminal OUT (node D) low. At this time, the output node E of the inverter INV2 is at a high level.

10 [0056]

When the input signal supplied to the input terminal (IN) of the buffer circuit falls at the timing  $T_A$  between the timings  $T_0$  and  $T_1$ , the output of the inverter INV1 changes from a low level to a high level, and two inputs to the NAND circuit NAND 1 (at the nodes B and E) both go to a high level. The node C which is the output node of the NAND circuit NAND1 goes to a low level, the PMOS transistor PM1 is turned on, and the output terminal OUT (node D) goes to a high level. A transition of the output terminal OUT to a high level causes the node E which is the output node of the inverter INV2 to undergo a transition to a low level. In response to the signal voltage (being at a high level) at the node B and the signal voltage (being at a low level) at the node E, the NAND circuit NAND1 causes the output node C to undergo a transition to a high level. The PMOS transistor PM1, to which a gate a high level is applied, is turned off. Since the input signal IN is at a low level at this time, the NMOS transistor NM1 and the PMOS transistor

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PM1 both are in an off state.

[0057]

The flip-flop composed of the inverters INV2 and INV3 stores and holds the logic value for the node D (logic level before a high-impedance state). During the period ( $T_{off}$ ) where the output terminal OUT of the buffer circuit is in a high-impedance state, the inverter INV3, the output terminal of which is set to a high level, charges the output terminal OUT of the buffer circuit, and functions to cause the output terminal OUT of the buffer circuit to go to a high level. The inverter V3 is composed of a CMOS inverter, and the size and the current driving capability of its PMOS transistor is made smaller than that of the PMOS transistor PM1 constituting the buffer circuit.

[0058]

If the output signal voltage of the output terminal OUT) (voltage at the node D) is at a high level( $V_{OH}$  or higher, where the  $V_{OH}$  is an output voltage HIGH), but does not reach the power supply voltage  $V_{DD}$  yet during the period where both of the PMOS transistor PM1 and the NMOS transistor NM1 in the buffer circuit are in an off state ( $T_{off}$  in Fig. 7), the output signal voltage of the output terminal (OUT) is pulled up to the power supply voltage  $V_{DD}$  by the inverter INV3 that outputs a high level.

[0059]

When the input signal IN undergoes a transition to a high level at the timing  $T_1$  in Fig. 7, the NMOS transistor NM1 is turned on. At this time, because the high level is applied to the gate of the PMOS transistor

PM1, the PMOS transistor PM1 is turned off, so that the output terminal OUT goes to a low level immediately. The duty ratio of the clock signal supplied to the input terminal (IN) of the buffer circuit in Fig. 7 is set to 1:1 (50%), for simplicity. In this embodiment, the duty ratio  
5 of the clock signal may, of course, be other than 1:1.

[0060]

Next, a third embodiment of the present invention will be described. Fig. 8 is a block diagram showing a configuration of the third embodiment of the present invention. As shown in Fig. 8, a  
10 buffer in this embodiment is obtained by cascading an inverting buffer circuit 10A and an inverting buffer circuit 10B and functions as an non-inverting buffer.

[0061]

The inverting buffer circuit 10A has the same structure as the  
15 buffer circuit in the first embodiment, described with reference to Fig. 1, and reduces a delay time from a fall of the input signal fed to the input terminal IN to a rise of the output signal. The inverting buffer circuit 10B has the same structure as the buffer circuit in the second embodiment, described with reference to Fig. 5, and reduces a delay  
20 time from a rise of the output signal of the inverting buffer circuit 10A to a fall of the output signal of the output terminal OUT.

[0062]

With this arrangement, the delay time from a fall of the input signal fed to the input terminal IN to a fall of the output signal of the  
25 output terminal OUT is reduced.

[0063]

When the inverting buffer circuit 10B is disposed in a front stage and the inverting buffer circuit 10A is disposed in a rear stage following the inverting buffer circuit 10B as a variation of this embodiment, the propagation delay time from a rise of the input signal fed to the input terminal IN to a fall of the output signal is reduced by the inverting buffer circuit 10B, and the propagation delay time from a fall of the output signal of the inverting buffer circuit 10B to a rise of the output signal of the output terminal OUT is reduced by the inverting buffer circuit 10A. With this arrangement, the propagation delay time from a rise of the input signal fed to the input terminal IN to a rise of the output signal of the output terminal OUT in the cascaded buffer circuits is reduced.

[0064]

Next, a fourth embodiment of the present invention will be described. Fig. 9 is a block diagram showing a configuration of the fourth embodiment of the present invention. In the configurations of the embodiments shown in Figs. 1 and 5, the flip-flop (composed of the inverters INV2 and INV3) is provided which sets the output terminal OUT of the buffer circuit to a low level or a high level that is the logic level immediately before the logic level of the output terminal OUT during the period  $T_{off}$  where the PMOS and NMOS transistors are both in an off state. Thus, the output terminal is thereby controlled to be at a normal logic level when the output terminal OUT of the buffer circuit is in an high-impedance state. However, when the period  $T_{off}$  in the

timing chart in Fig. 4, for example, where the output terminal OUT of the buffer circuit is in the high-impedance state, is comparatively short, an effect of the present invention can be achieved to a certain degree even if the flip-flop constituted from the inverters INV2 and INV3, shown in Figs. 1 and 5, is omitted. In other words, if the period  $T_{off}$  is short, there is little possibility that an erroneous logic level of the output terminal OUT of the buffer circuit is passed on to a subsequent circuit. In this case, referring to Fig. 9, a gate of a PMOS transistor PM1 is connected to an input terminal IN, and a gate of an NMOS transistor NM1 is connected to an output terminal of a NOR circuit NOR1. The NOR circuit NOR1 receives an output of the inverter INV1 that receives and inverts the input signal fed to the input terminal IN and the output of a delay circuit 100 that receives and delays the input signal fed to the input terminal IN.

15 [0065]

In the present embodiment, a rise transition of the signal of the output terminal OUT in the buffer circuit from a low level to a high level during a fall of the input signal fed to the input terminal IN of the buffer circuit from a high level to a low level is the same as a timing waveform shown in Fig. 3.

[0066]

Fig. 10 is a timing chart showing an operation of the fourth embodiment of the present invention. In this embodiment, when the input signal fed to the input terminal IN rises from a low level to a high level (at  $T_0$ ), the node B which is an output node of the inverter INV1

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goes to a low level, in response to the transition of the input signal. At this time, because the output signal of the delay circuit 100 is still at a low level (a high-level signal is not outputted to the node E), the NOR circuit NOR1, which receives a low level at the node E, changes the output node C to a high level, in response to the transition of the node B to the low level. When the node C goes to a high level, the NMOS transistor NM1 is turned on, so that the output terminal OUT goes to a low level.

[0067]

The delay circuit 100 that receives the input signal from the input terminal IN delays a rise of the input signal by a time  $t_{d1}$ , and outputs the delayed signal to the node E, which is the output terminal of the delay circuit 100. The NOR circuit NOR1 changes the node C from a high to a low level, in response to the rise transition of the node E from a low level to a high level. As a result, the NMOS transistor NM1 is turned off. At this time, the signal fed to the input terminal IN is at a high level, and the PMOS transistor PM1 and the NMOS transistor NM1 are both in an off state (refer to the period  $T_{off}$  in Fig. 10).

[0068]

Then, at the timing  $T_A$  in Fig. 10, the input signal IN goes from a high level to a low level, the PMOS transistor PM1 is turned on, and the output terminal OUT goes to a high level. By adjusting the delay time of the delay circuit 100 to reduce the period  $T_{off}$ , the circuit for setting the output terminal OUT to a logic value immediately before the output terminal OUT is set in a high-impedance state, with the output terminal

OUT being kept in the high-impedance state for a long time, becomes unnecessary. Incidentally, in this fourth embodiment, the flip-flop composed of two inverters (INV2 and INV3) may of course be connected to the output terminal OUT of the buffer circuit, as in the first and second embodiments. Incidentally, in Fig. 10, a timing of a fall transition of the clock signal supplied to the input terminal (IN) of the buffer circuit from a high level to a low level between the timings  $T_0$  and  $T_1$  is indicated by  $T_A$ , and the duty ratio of the clock signal supplied to the input terminal (IN) of the buffer circuit is set to 1:1 (50%), for simplicity. In this embodiment, the duty ratio of the clock signal may, of course, be other than 1:1.

[0069]

The delay circuit 100 in Fig. 9 may be composed of a delay locked loop (DLL) as shown in Fig. 11, for example. That is, the delay circuit 100 includes a delay circuit 101 for receiving and then delaying an input signal, with its delay time made adjustable, a delay replica 103 for receiving and then delaying the output of the delay circuit 101 by a predetermined delay time, and a phase detection circuit 102 for comparing a phase of the output of the delay replica 103 with a phase of the input signal. The delay time of the delay circuit 101 is variably set, based on a result of detection by the phase detection circuit 102.

[0070]

A rising edge of an input signal in a certain clock cycle is delayed by a delay time  $td1$  at the delay circuit 101, and also delayed by a delay time  $td2$  at the delay replica 103. At the phase detection circuit 102,

the delay time of the delay circuit 101 is adjusted so that the phase of the rising edge of a signal in a subsequent cycle coincides with the phase of the output signal of the delay replica 103.

[0071]

5           When the signal (clock) fed to the input terminal IN is a clock signal with a cycle  $t_{CK}$  and a duty of 50% and the delay time of the delay replica 103 is set to  $td2$ , the delay time  $td1$  of the delay circuit 101 is given by an equation:

$$td1 = t_{CK} - td2,$$

10           and the off period  $T_{off}$  is given by an equation:

$$T_{off} = td2 - t_{CK}/2.$$

By setting the delay time  $td2$  of the delay replica based on a typical value of the off period  $T_{off}$ , the node C is set to a low level by the period  $T_{off}$  earlier with respect to a falling edge of the signal fed to the input terminal IN. Thus, when the PMOS transistor PM1 is turned on in response to a fall of the signal fed to the input terminal IN, the NMOS transistor NM1 is kept off.

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[0072]

In this embodiment, the delay circuit 100 is not limited to a DLL circuit. A synchronous type delay circuit that includes a first row of delay circuits and a second row of delay circuits with their clock propagation directions opposite to each other may also be employed. In this circuit, a clock pulse that has proceeded through the first row of the delay circuits is transferred to the second row of the delay circuits through a transfer circuit in response to a subsequent clock pulse in a

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direction opposite to the direction in which the clock pulse proceeded through the first row of the delay circuits.

[0073]

When the buffer circuits of the present invention are incorporated  
5 into a semiconductor integrated circuit as clock tree buffers, a configuration becomes the one as shown in Fig. 12, for example. When flip-flops (or registers) FF1 through FF12 are configured to sample data at a rising edge of a clock, and four inverters are inserted into a clock tree, INV101 and INV103 to INV105 are composed of the inverting  
10 buffers shown in Fig. 5, and INV102 and INV106 to INV117 are composed of the inverting buffers shown in Fig. 1.

[0074]

Next, a case where performance of clock tree buffers that use the buffer circuits according to the present invention was compared with  
15 performance of clock tree buffers that use conventional CMOS inverters to perform evaluation(benchmark) will be described. Fig. 14 is a graph as a comparison example, showing an input waveform IN1 and an output waveform DOUT1 resulting from a transient analysis simulation when inverting buffers composed of ordinary CMOS inverters were employed  
20 for two inverters INV101 and INV102 in Fig.12. A ratio  $\beta_p/\beta_n$  of a gain coefficient  $\beta$  of the PMOS transistor to the gain coefficient  $\beta$  of the NMOS transistor at a first inverter in Fig. 12 is set to 150/75, while the ratio  $\beta_p/\beta_n$  of the gain coefficient  $\beta$  of the PMOS transistor to the gain coefficient  $\beta$  of the NMOS transistor at a second inverter in Fig. 12 is  
25 set to 400/200.

[0075]

A signal from a receiver circuit (a differential inverting buffer circuit), not shown, is assumed to be supplied to the first CMOS inverter INV101 in Fig. 12. A minimum amplitude value and a maximum amplitude value of a signal (IN1) supplied to the receiver circuit is set  
 5 to 0.25V and 1.25V, respectively. The clock cycle tCK is set to 3 ns, the duty ratio is set to 3:2, and a rise time is set to 0.3 ns. As shown in Fig. 14, the propagation delay time from a rise of the input signal IN1 to a fall of an output signal DOUT1 (in Fig. 12) that is the output of the  
 10 CMOS inverter INV103 is 0.5456 ns ( $\approx$  545 ps), and the propagation delay time from a fall of the input signal IN1 to a rise of the output signal DOUT1 is 0.5252 ns ( $\approx$  525 ps).

[0076]

On the other hand, Fig. 13 is a graph showing the input waveform  
 15 IN1 and the output waveform DOUT1 resulting from the transient analysis simulation when the buffer circuit 10B and the buffer circuit 10A shown in Fig. 8, according to the embodiment of the present invention are employed as the two inverters INV101 and INV102, respectively, in Fig.12. The input terminal of the inverter INV101 in  
 20 Fig. 12 is assumed to receive the output signal of the receiver circuit (inverting buffer circuit), not shown. The minimum amplitude value and the maximum amplitude value of the signal (IN1) supplied to the receiver circuit are set to 0.25V and 1.25V, respectively. The clock cycle tCK is set to 3 ns, the duty ratio is set to 3:2, and the rise time is  
 25 set to 0.3 ns. The  $\beta_p/\beta_n$  of the first buffer circuit 10A (ratio of the gain

coefficient  $\beta$  of the PMOS transistor PM11 to the gain coefficient  $\beta$  of the NMOS transistor NM11) is set to 180/80, while the  $\beta_p/\beta_n$  of the second buffer circuit 10B (ratio of the gain coefficient  $\beta$  of the PMOS transistor PM12 to the gain coefficient  $\beta$  of the NMOS transistor NM12) is set to 100/150. The propagation delay time from a rise of the input signal IN1 to a fall of the output signal DOUT1 (in Fig. 12) is 0.4814 ns ( $\approx$  481 ps), and the propagation delay time from a fall of the input signal IN1 to a rise of the output signal DOUT1 (in Fig. 12) is 0.8336 ns ( $\approx$  833 ps).

10 [0077]

Referring to Fig. 13, the off period (a period where the DOUT1 is at a high level) is set to 0.8441 ns (844.1 ps). During this off period, in the buffer circuit 10B in Fig. 8, which constitutes the buffer INV102 in Fig. 12, the PMOS transistor PM12 is in an off state, (the NMOS transistor NM12 is also in an off state, and the output of the buffer circuit 10B is in a high-impedance state). Using the output of an inverter INV15 that constitutes a flip-flop, the output terminal OUT of the buffer circuit 10B in the off state is pulled up to the power supply voltage VDD. Based on comparison between these analysis results, the propagation delay time  $t_{pLH}$  from a fall of the input fed to the receiver circuit to a rise of the output (DOUT1) in this embodiment is 481 ps, which is approximately 12% shorter than in the case of the configuration constituted from the conventional CMOS inverters.

20 [0078]

25 Still another embodiment of the present invention will be

described. Fig. 15 is a block diagram showing a configuration of a fifth embodiment of the present invention, and shows a variation of the first embodiment shown in Fig. 1. That is, referring to Fig. 15, a buffer circuit in the fifth embodiment of the present invention is configured by replacing the two-input NOR circuit NOR1 that receives the outputs of the inverter INV1 and the inverter INV2 in Fig. 1 with a three-input NOR circuit NOR3. The output signal of the inverter INV1, the output signal of the inverter INV2, and a selection control signal supplied from an outside of the buffer circuit are fed to three respective input terminals of the three-input NOR circuit NOR3. The configuration other than this is the same as that in the first embodiment.

[0079]

An operation of the fifth embodiment of the present invention will be described below. When the selection control signal is at a high level, so as to deactivate the buffer circuit, the output of the three-input NOR circuit NOR3 is forcibly set to a low level, irrespective of values of other two input signals (other two input signals are masked). The NMOS transistor NM1 that receives the output signal of the three-input NOR circuit NOR3 at its gate is turned off irrespective of the value of the signal supplied to the input terminal IN. When the selection control signal goes to a high level, the NMOS transistor NM1 is kept from being turned on in this manner. Thus, the node D is fixed at a high level. That is, an output of the clock signal supplied to the input terminal IN of the buffer circuit is stopped.

[0080]

On the other hand, when the selection control signal goes to a low level to activate the buffer circuit in the fifth embodiment of the present invention, the same operation as in the embodiment described with reference to Fig. 1 is performed. That is, when the selection control  
5 signal is at a low level, the three-input NOR circuit NOR3 outputs a high level when the values of other two input terminals, or the values of the output signals of the inverter INV1 and the inverter INV2 are both at a low level, (when the signals of the input terminal IN and the output terminal OUT are both at a high level). The NMOS transistor NM1 is  
10 thus turned on, and the node D goes to a low level. As a result, the output signal of the inverter INV2 goes to a high level, the three-input NOR circuit NOR3 outputs a low level to turn off the NMOS transistor NM1. When the input signal supplied to the input terminal IN goes to a low level, the PMOS transistor PM1 is switched on to charge the node D.  
15 At this time, the output signal of the inverter INV1 goes to a high level, the three-input NOR circuit NOR3 outputs a low level, and the NMOS transistor NM1 is kept off. Since the PMOS transistor PM1 is switched on while the NMOS transistor NM1 is kept off in this manner, the short-circuit current from the high-potential power supply VDD to the  
20 low-potential power supply VSS does not flow. Power consumption is thereby reduced, and the output terminal is charged at high speed. Since the fifth embodiment of the present invention can stop clocking as necessary while keeping high-speed supply of a high-level output, it is suited for being applied to a semiconductor device or the like that has  
25 a power saving function such as a standby mode.

[0081]

Fig. 16 is a block diagram showing a configuration of a sixth embodiment of the present invention. The sixth embodiment of the present invention is a variation of the second embodiment described with reference to Fig. 5. That is, referring to Fig. 16, the sixth embodiment of the present invention is obtained by replacing the two-input NAND circuit NAND1 in Fig. 5 with a three-input NAND circuit NAND3. The output signal of the inverter INV1, the output signal of the inverter INV2, and the inverted signal of the selection control signal in Fig. 15 are input to the three respective input terminals of the three-input NAND circuit NAND3. The configuration other than this is the same as that in the second embodiment. In an example shown in Fig. 16, the selection control signal is used in common with the one shown in Fig. 15. Thus, the inverted signal of the selection control signal is input to the three-input NAND circuit NAND3. However, logic of the selection control signal can be arbitrarily set. If the logic levels of the selection control signal for activating and deactivating the buffer circuit in Fig. 16 are set to the high level and the low level, respectively, which are different from the example shown in Fig. 15, the selection control signal is supplied to the three-input NAND circuit NAND3.

[0082]

An operation of the sixth embodiment of the present invention will be described below. When the selection control signal is set to a high level so as to deactivate the buffer circuit, the inverted signal of the selection control signal to be supplied to the three-input NAND

circuit NAND3 goes to a low level. Then, the three-input NAND circuit NAND3 outputs a high level to turns off the PMOS transistor PM1. Since the PMOS transistor PM1 is kept from being turned on, the node D is fixed at a low level. That is, output of the clock signal supplied to the input terminal of the buffer circuit is stopped.

[0083]

On the other hand, when the selection control signal is set to a low level so as to activate the buffer circuit, the same operation as in the embodiment described with reference to Fig. 5 is performed. That is, when the selection control signal is at a low level, the three-input NAND circuit NAND3 that receives its inverted signal outputs a low level if the values of other two input terminals or the values of the output signals of the inverters INV1 and INV2 are both at a high level (when the signals of the input terminal IN and the output terminal OUT are both at a low level). The PMOS transistor is thus turned on, and the node D goes to a high level. As a result, the output signal of the inverter INV2 goes to a low level, and the three-input NAND circuit NAND3 outputs a high level to turn off the PMOS transistor PM1. When the input signal supplied to the input terminal IN goes to a high level, the NMOS transistor NM1 is switched on to discharge the node D. At this time, the output signal of the inverter INV1 goes to a low level, and the three-input NANA circuit NAND3 outputs a high level. The PMOS transistor PM1 is thus kept off. Since the NMOS transistor NM1 is switched from off to on with the PMOS transistor PM1 being kept off in this manner, the short-circuit current from the high-potential power supply VDD to the low-potential

power supply VSS does not flow. Current consumption is thereby reduced, and the output terminal is discharged at high speed. Since this embodiment can stop clock supply as necessary while keeping high-speed supply of a low-level output, it is ideal for being applied to the semiconductor device or the like that has the power saving function such as the standby mode. Incidentally, either one or both of the NOR3 in the fifth embodiment of the present invention and the NAND 3 in the sixth embodiment of the present invention, shown in Fig. 15 and Fig. 16, respectively, may of course be applied to either one or both of the buffer circuits 10A and 10B in Fig. 8. The two-input NOR circuit NOR1 shown in Fig. 9 may of course be replaced with the three-input NOR circuit that further receives the selection control signal.

[0084]

The foregoing descriptions were made in conjunction with the embodiments. The present invention, however, is not limited to the embodiments described above, and naturally includes various variations and modifications that could be made by those skilled in the art within the scope of the claims of the present invention.

[0085]

The meritorious effects of the present invention are summarized as follows.

As described above, according to the buffer circuit of the present invention, a propagation delay time of a signal is reduced. When a buffer for delay adjustment according to the buffer circuit of the present invention is inserted into a clock path, an effect of the delay adjustment



buffer on a timing margin for a clock destination is alleviated. The buffer circuit of the present invention is thus ideal for use in a buffer tree or the like equipped with a semiconductor integrated circuit. Further, the buffer circuit of the present invention can control  
5 propagation and stop of a signal based on a control signal for controlling activation/deactivation while maintaining a reduction in the delay time of the signal. The buffer circuit of the present invention is thus ideal for use in a buffer tree circuit in a high-speed semiconductor device with a power saving function or the like.

10 It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed  
15 and/or claimed elements, matters and/or items may fall under the modifications aforementioned.